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Integrated acoustic resonators in commercial fin field-effect transistor technology

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In radio communication, the growth of beamforming and multiple-input-multiple-output technologies, which increase transceiver complexity, have led to a drive to reduce the size, weight and power of radio components by integrating them into a single system on chip. One approach is to integrate the frequency references of acoustic microelectromechanical systems (MEMS) with complementary metal-oxide-semiconductor processes, typically through a MEMS-first or MEMS-last approach that requires process customization. Here we report unreleased acoustic resonators that are fabricated in 14 nm fin field-effect transistor technology and operate in the X-band frequency range (8–12 GHz). The devices use phononic waveguides for acoustic confinement and exploit metal-oxide-semiconductor capacitors and transistors to electromechanically drive and sense acoustic vibrations. Fifteen device variations are analysed across 30 bias points, quantifying the importance of phononic confinement on resonator performance and demonstrating the velocity-saturated piezoresistive effect in active resonant transistors. Our results illustrate the feasibility of integrating acoustic devices directly into standard complementary metal-oxide-semiconductor processes.

There is currently an increased focus on the functional diversification of existing semiconductor process nodes to create new technologies^{1,2}. This approach increases performance, supply chain resilience and security by reducing the number of chips from different process technologies that must be integrated and packaged into the final product. For technologies such as the fifth generation of wireless communications technology, such innovation is necessary to enable high-performance adaptable radios, where high-frequency resonators are a key element in both filters and voltage-controlled oscillators used. Recent developments in this area include thin-film bulk acoustic resonators with ferroelectric materials, as well as high-frequency Lamb- and Lamé-wave resonators using piezoelectric lithium niobate or aluminium nitride thin films^{3–6}.

To address band congestion, multiple-input-multiple-output arrays are becoming increasingly common as a way to multiplex transmissions between users in the same band, with large arrays allowing for increased performance across end users sharing the spectrum⁷. The beamforming enabled by such an antenna array is of particular use for higher-frequency bands, where propagation conditions are less stable due to increased radio-frequency (RF) absorption. These RF front ends require many more analogue components to be integrated in a compact form factor, driving research in RF integration into traditional digital processes.

Many high-performance technologies require integration using microelectromechanical systems (MEMS)-first or MEMS-last process schemes^{8–10}, which provide space and power savings compared with off-chip RF integration. The use of phononic-crystal (PnC) confinement, however, could allow resonator integration directly into a standard complementary metal-oxide-semiconductor (CMOS) process, potentially leading to larger multiple-input-multiple-output arrays in a smaller footprint at lower power^{11,12}. In addition to reducing parasitics from routing high-frequency signals over long distances, this also provides the opportunity to use high-performance transistors for active transduction, leading to potentially enhanced performance. Such an approach also provides

a route to future acoustic coupling between devices co-located on the same chip, which reduces the need for power-hungry phase-locked loops and allows scaled coupled oscillator systems for neuromorphic computing to be explored^{13–16}. In this Article, we report CMOS fin field-effect transistor (FinFET)-based resonators that utilize acoustic waveguiding confinement operating in the Institute of Electrical and Electronics Engineers (IEEE) X-band of 8–12 GHz.

Resonator cavity design

The designed resonator structure, referred to as a fin resonant body transistor (fRBT) (Fig. 1), is fully integrated in the GlobalFoundries 14LPP commercial process and occupies a space of $9\mu\text{m} \times 15\mu\text{m}$ (ref. 17). The device is a four-port network, differentially driven between adjacent gates along the fin length with the output of the resonator taken as the differential transconductance (equation (1)), which is a function of three main items: the electrical-to-acoustic transduction efficiency in the drive transistors, acoustic energy confinement and amplification in the resonance cavity, and acoustic-to-drain current conversion in the output transistors. The first of these items, namely, drive transduction, is electrostatic due to the 14 nm fabrication process used, although the potential exists for future piezoelectric drive using CMOS-compatible thin-film ferroelectrics^{4,18,19}. The third item, namely, acoustic-to-drain current conversion, is also largely a function of the process and materials used in device fabrication. Although this conversion will be examined utilizing a simplified model, the initial device design is focused on maximizing the acoustic energy confinement by varying the gate length, termination scheme and back-end-of-line (BEOL) confinement conditions:

$$g_{\text{mdd}} = \frac{i_d}{v_d} = Y_{\text{dd}21} - Y_{\text{dd}12}. \quad (1)$$

Figure 1a depicts a three-dimensional (3D) unit cell of the resonator with a 14-nm-wide FinFET at the front-end-of-line (FEOL)

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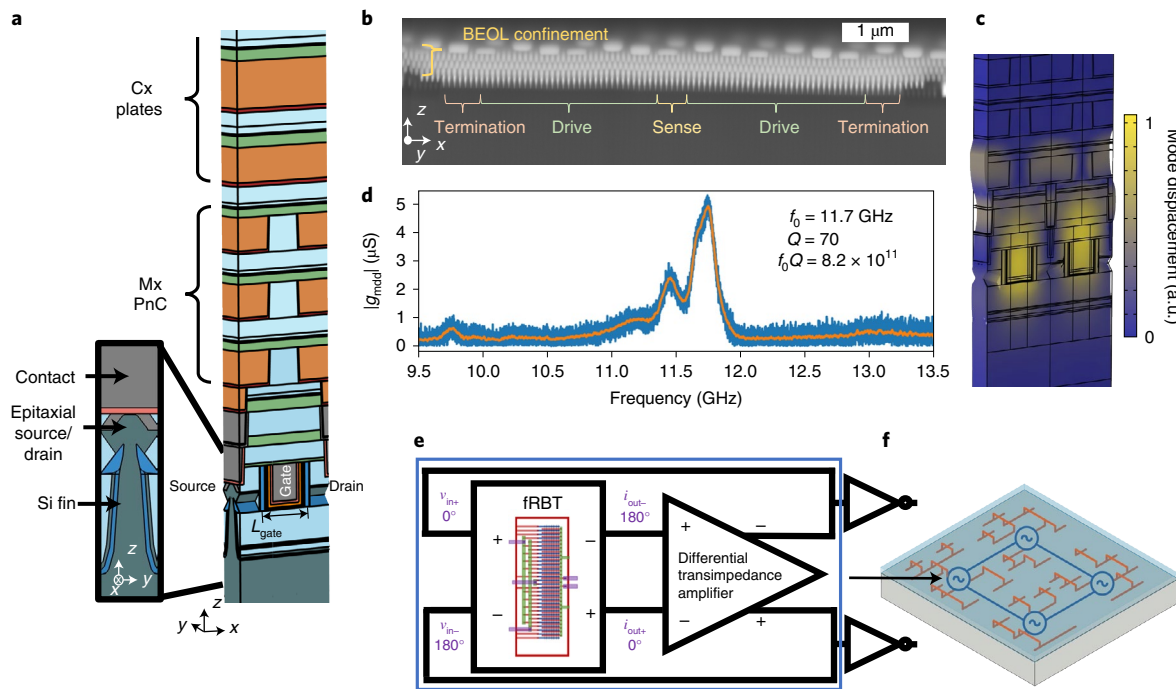


Fig. 1 | Overview of FinFET resonator. **a**, Cross-section of one period of the FinFET resonator, modelled in COMSOL, with the inset highlighting the Si fin (dark green) and epitaxial raised source and drain with silicide²⁰. The metal and contact layers are highlighted in orange and dark grey, respectively, and the dielectric layers are coloured blue and green. The target mode is primarily defined along the x direction (L_{gate}) via the 180° -phase constraint due to the differential drive and sense. **b**, Representative acoustic cavity, consisting of a sense block sandwiched between two drive blocks, with terminations at either end to increase acoustic confinement. A differential input is applied in the two drive blocks, with the output current taken from the sense transistors at the centre of the cavity. The grounded gates act as electrical isolation between the sense and drive blocks. **c**, Simulated target mode, with periodicity driven by L_{gate} showing stress concentrated in the FinFET channel and confined by the BEOL metal layers. **d**, Experimentally measured mode, with $f_0 Q$ product of 8.2×10^{11} , placing it within an order of magnitude of the released MEMS resonators. **e**, Combined with a differential transconductance amplifier, the fRBT enables a high-frequency mechanically referenced two-phase oscillator in the standard CMOS process. Oscillator design considerations for active transduction resonators are presented elsewhere³⁹. **f**, Acoustically coupled (blue lines) network of oscillators in CMOS FEOL with local electrical clock routing (bronze lines), eliminating power-hungry phase-locked loops used for clock distribution. This could also enable scalable oscillatory computing for neuromorphic applications, directly interfaced with a classical CMOS circuit.

condition and periodically arranged metal blocks at the BEOL, categorized into Mx and Cx layers shown based on the thickness and minimum lateral feature sizes (Fig. 2a). The target resonant mode for the unreleased resonator is along the length direction of the fin transistors. To obtain a lower insertion loss and higher quality (Q) factor, the radiated acoustic energy needs to be concentrated at the metal–oxide–semiconductor capacitor drive transducers and sensing transistors. Compared with more traditional suspended resonators, this represents a challenge in the unreleased resonant body transistor design in commercial CMOS processes.

Integrating a PnC at the BEOL of the standard CMOS process and leveraging the mechanical bandgaps of such structures has proven to be an effective tool to confine the energy and boost the resonance Q factor^{4,12}. As shown by M1 in Fig. 3a, these periodic metals are uniform along the length (y direction) of the transistor gates (orthogonal to the fin direction) within the resonant cavity.

To study and optimize the bandgap induced by the PnCs, several 3D simulations were performed in COMSOL Multiphysics²⁰. Specifically, by mapping the real coordinates to reciprocal coordinates and searching for the eigenmodes along the first irreducible Brillouin zone in the 3D reciprocal lattice, a $130 \times 60 \text{ nm}^2$ PnC (such as one that can be designed within the constraints of the Mx layers in the 14 nm process) yields a partial bandgap at the operating point (X) from 9.0 to 14.0 GHz (complete from 11.9 to 12.5 GHz; Fig. 2d). For the longer 106-nm-gate-length device, the design rules are such that a $76 \times 32 \text{ nm}^2$ PnC can be utilized with two periods per unit cell.

This smaller periodicity of PnC leads to complete bandgaps (Fig. 2b) from 8.7 to 9.9 GHz and from 12.3 to 14.6 GHz. At X, partial bandgaps exist from 8.2 to 12.0 GHz and from 12.0 to 14.6 GHz.

To further confine the elastic energy, a separate PnC designed under the design rules of the Cx metal layer is also considered for a subset of devices. The corresponding dispersion relationship is shown in Fig. 2c. A complete mechanical bandgap is then obtained between 8.7 and 9.8 GHz (a partial one from 9.8 to 11.8 GHz at X), which overlaps with the bandgap induced by the Mx metal PnC. Together, these PnC designs indicate that elastic waves with a frequency of 9–14 GHz propagating along the fin can be prohibited from propagating into the BEOL, with a subset of that frequency range experiencing a complete bandgap. For this reason, the devices are designed for a waveguided mode with a differential drive that exhibits a large momentum ($k_x = \pi/a$) at a frequency below the sound cone for the bulk silicon substrate, laterally confining the mode towards the driving/sensing transistors¹². When the design rules do not allow fine-pitched PnCs, continuous metal plates may be used as acoustic Bragg reflectors, although their translational symmetry in two dimensions can only lead to partial bandgaps (Fig. 2e,f)²¹.

Although the PnCs in the main resonant cavity enhance energy confinement and wave reflection from the BEOL, there also exists wave scattering at the two ends of the resonator. Reducing this scattering further increases the horizontal confinement, reduces the insertion loss, and hence increases the Q . The adiabatic theorem in photonic-waveguide design is leveraged here, which states that

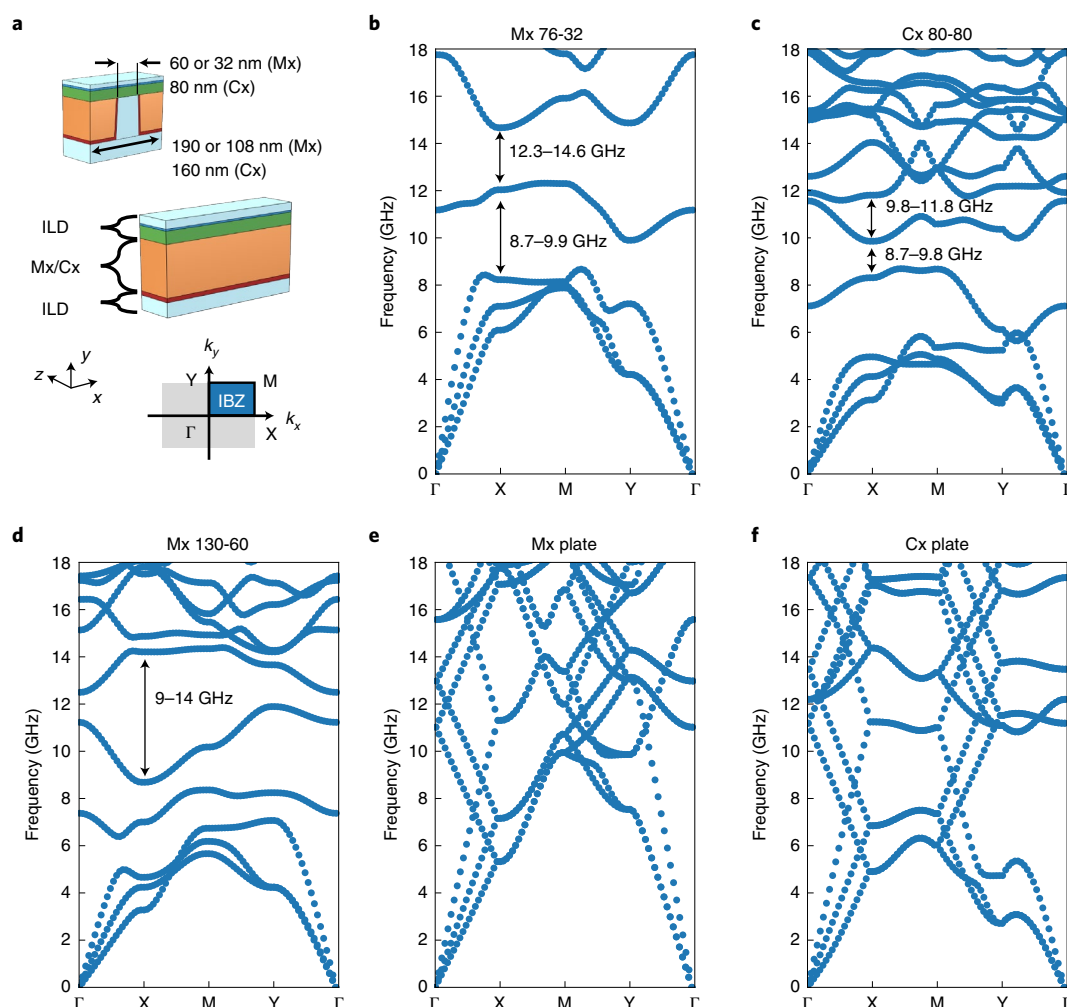


Fig. 2 | BEOL acoustic confinement. **a**, Representative unit cell for the simulated periodic PnC and plate structures (Mx 76-32 and Cx plates are shown), including the metal layer and interlayer dielectric (ILD) films present between each metal layer. The orange region represents the metal, whereas the surrounding layers are the dielectric. These structures extend throughout the width of the cavity ($k_z = 0$); hence, the band structure is shown over the irreducible Brillouin zone (IBZ) for a two-dimensional (2D) rectangular lattice, with x and y directions chosen to give the typical lattice points. Note that this swaps the y and z dimensions from the 3D device coordinates given in Fig. 1. The thickness of each layer is set by the process technology and varies between the Mx and Cx layers. **b,c**, Dispersion relationships for the 108 nm periodic PnC (**b**, utilized in $L_{\text{gate}} = 106$ nm devices with two PnC unit cells per device unit cell) along with the upper (Cx) metal layer of the 160 nm periodic PnC (**c**, utilized in all the unit cells). **d-f**, Dispersion relationship for Mx 130-60 PnCs (**d**, 190 nm periodic), utilized in $L_{\text{gate}} = 80$ nm devices, along with the Mx (**e**) and Cx (**f**) plate geometries. As expected, the plates show no complete bandgap over two dimensions, with propagation of the waveguided modes possible in the x direction. PnC arrangements, although exhibiting waveguided modes in the z direction, still have complete bandgaps in the x and y dimensions. Due to continuous translation symmetry in the plates, the periodicity (and hence the definition of periodic cell dimension a and point X) is somewhat arbitrary. The frequency at which these propagating modes reach the X point depends on the definition of X, with the dispersion relations in **e** and **f** corresponding to a width of 190 nm (for $L_{\text{gate}} = 80$ nm devices). Longer L_{gate} devices will have a smaller relative momentum and hence will reach the X point at lower frequencies, as evident from the dispersion relations in Fig. 4.

when the wave is propagated down the waveguide, scattering vanishes because of the limitation of sufficiently slow perturbation²¹. Therefore, the key to reduce this scattering is to introduce different units as terminations at the two ends for slower transitions. The unit cell for all the PnC structures in the major termination section throughout the paper is kept as $150 \text{ nm} \times 60 \text{ nm}$.

Although all the measured devices have ten terminating gates at each end of the cavity, two types of cavity termination spacing are explored to provide acoustic confinement in the lateral direction, namely, abrupt and gradual termination schemes (Fig. 3b). Abrupt termination refers to the scenario where a terminating periodic array with a constant pitch shifted from that of the resonance cavity array is immediately adjacent to the main resonance region. In this case, the gate length of the termination immediately transitions

to the L_{term} value (Fig. 3d) and stays constant until the end of the device. As such, the guided waves are abruptly transitioned from the main cavity towards the ends. In the gradual termination scenario, the periodicity of the main resonant cavity adiabatically transitions from L_{gate} to the periodicity of the terminating array (L_{term}), resulting in a termination gate length gradually transitioning from 80 to 140 nm. This serves to reduce scattering from the two ends and boost Q (ref. 12).

FinFET active sensing

To understand the conversion from stress to drain current in the sense transistors, the modulation of three separate FET properties is examined: oxide capacitance, channel mobility due to piezoresistivity, and silicon bandgap. For ease of visualization, an initial analysis

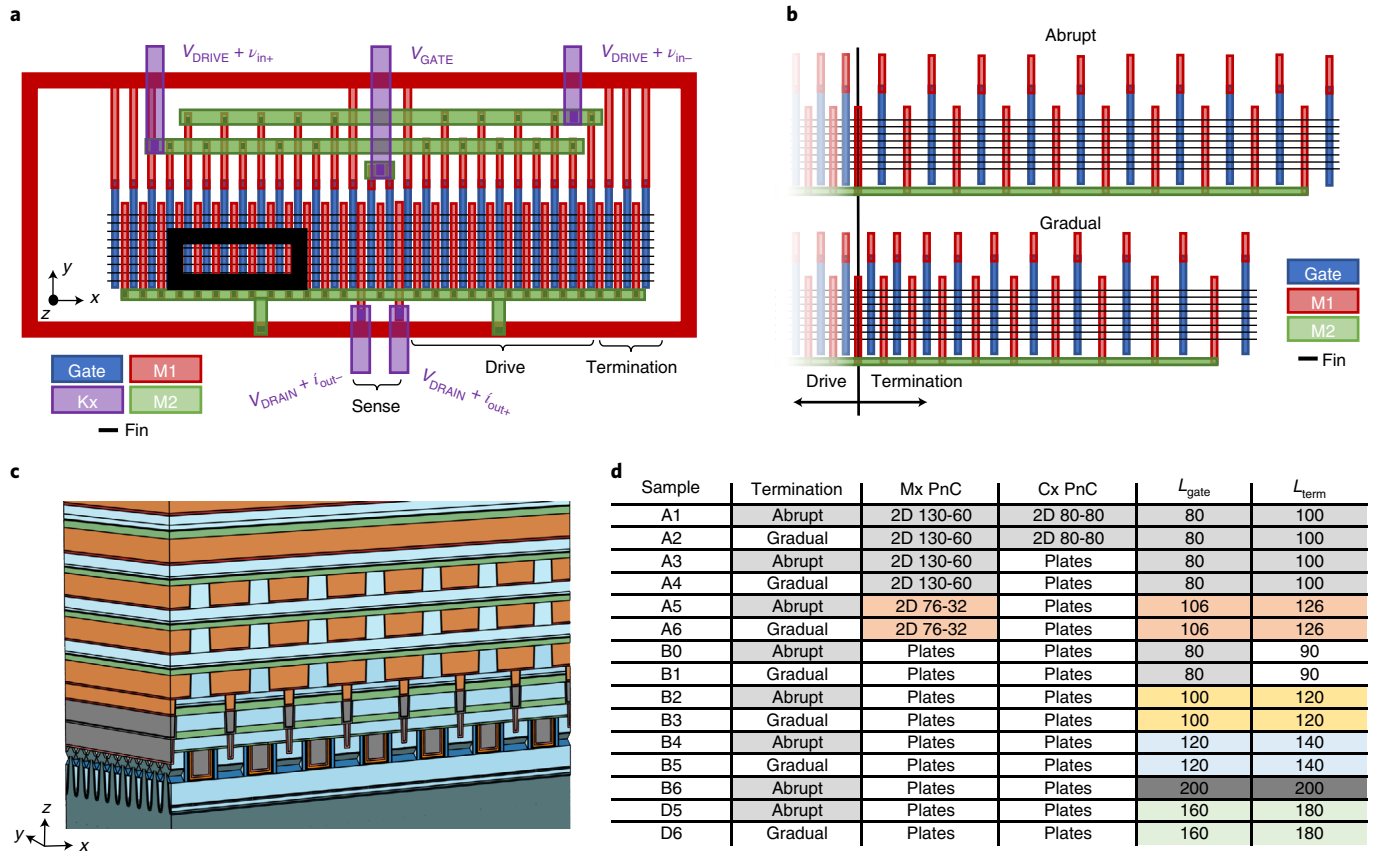


Fig. 3 | Variations in resonant cavity design. **a**, Top-down view of the device shows the central sense transistors with five pairs of capacitors on either side, allowing for a differential drive, capped on either end by termination (ten gates in the actual devices, abbreviated to three in the figure) and surrounded by a ground ring. The first-level metal M1 is used for routing within the structure, whereas higher-level metals in Mx and Cx (not shown for clarity in this diagram) rest above this routing in either the continuous plate or the PnC form. The Kx layer represents higher-level metal layers used for device-to-pad routing. **b**, Depiction of termination schemes investigated for use at the ends of the resonant cavity. **c**, View of a subset of the resonant cavity of devices A3 and A4, showing fins extending in the x direction and gates extending into the y direction. The RF drive signal is differentially applied, with alternating gates 180° out of phase. **d**, Variations in device design that were implemented and tested.

is performed with the source-referenced simplified strong-inversion model with $\alpha=1$ (the traditional ‘square-law model’ or SPICE level 1)²²:

$$I_{d0} = \mu_0 C_{ox0} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right), \quad (2)$$

where I_d is the drain current; μ is the carrier mobility; C_{ox} is the gate capacitance; V_{DS} and V_{GS} are the drain-to-source and gate-to-source bias, respectively; W and L are the channel width and length, respectively; and V_T is the threshold voltage required for substantial channel conduction.

This model has only a handful of parameters to describe the device operation, as opposed to the more advanced BSIM model commonly used in industry (Supplementary Information), which includes many empirically fit parameters to give the best device models for commercial applications²³. Additional information on the methods to simulate FRBTs in BSIM using a commercial process design kit is provided elsewhere²⁴.

Capacitance modulation in these devices is the same mechanism used in the electrostatic drive of these devices, except that rather than directly sensing the gate current, the capacitance modulation is being amplified through transistor action into a change in drain current. The piezoresistive effect, where the semiconductor carrier mobility is modulated through stress in the transistor channel,

similarly appears as a multiplier on the transistor drain current. Modulation of semiconductor bandgap, on the other hand, largely affects the threshold voltage of the transistor. Supplementary Section 1 provides a complete derivation of these effects. Modified to include the effects of stress on μ , C_{ox} and V_T (modelled as $\mu(\sigma) = \mu_0 + \Delta\mu$), the original expression for current in the linear region becomes the following:

$$I_d(\sigma) = (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta\mu + \Delta\mu \Delta C_{ox}) \times \frac{W}{L} \left((V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right) - \Delta V_T V_{DS} \frac{W}{L} (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta\mu + \Delta\mu \Delta C_{ox}), \quad (3)$$

where

$$\Delta I_d(\sigma) = (\mu_0 \Delta C_{ox} + C_{ox0} \Delta\mu + \Delta\mu \Delta C_{ox}) \times \frac{W}{L} \left((V_{GS} - V_{T0}) V_{DS} - \frac{V_{DS}^2}{2} \right) - \Delta V_T V_{DS} \frac{W}{L} (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta\mu + \Delta\mu \Delta C_{ox}). \quad (4)$$

Similarly, in saturation,

$$I_{d0} = \mu_0 C_{ox0} \frac{W}{L} ((V_{GS} - V_T)^2 (1 + \lambda[V_{DS} - (V_{GS} - V_{T0})])), \quad (5)$$

where λ represents the channel-length modulation coefficient (typically, 0.05 to 0.25) and

$$\begin{aligned} \Delta I_d = & (\mu_0 \Delta C_{ox} + C_{ox0} \Delta \mu + \Delta \mu \Delta C_{ox}) \\ & \times \frac{W}{2L} ((V_{GS} - V_T)^2 (1 + \lambda(V_{DS} - V_{GS} + V_T))) \\ & - \frac{W}{2L} (\mu_0 C_{ox0} + \mu_0 \Delta C_{ox} + C_{ox0} \Delta \mu + \Delta \mu \Delta C_{ox}) \\ & [\Delta V_T [\lambda(V_{GS} - V_{T0})^2 - 2(V_{GS} - V_{T0}) \times \\ & (1 + \lambda[V_{DS} - (V_{GS} - V_{T0})])] \\ & + \Delta V_T^2 [(1 + \lambda[V_{DS} - (V_{GS} - V_{T0})]) - 2\lambda(V_{GS} - V_{T0})] \\ & + \Delta V_T^3 [\lambda]] \end{aligned} \quad (6)$$

For modern submicron devices, carriers do not exhibit constant mobility, but rather undergo velocity saturation at high fields. A simplified way to analytically model this is through a piecewise equation involving the saturation field (E_{sat}) and lateral field (E_x) in the direction of carrier motion as

$$v_d = \begin{cases} \frac{\mu |E_x|}{1 + |E_x|/E_{sat}}, & |E_x| < E_{sat} \\ v_{sat}, & |E_x| > E_{sat} \end{cases}, \quad (7)$$

which, solved at $v_d = v_{sat}$, gives

$$E_{sat} = \frac{2v_{sat}}{\mu} \quad (8)$$

and leads to a modified expression for drain current, namely,

$$I_{d0} = \begin{cases} \mu_0 C_{ox0} \frac{W}{L} \frac{1}{1 + \frac{V_{DS}}{E_{sat}L}} ((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}), & V_{DS} < V_{DSsat} \\ C_{ox0} W v_{sat0} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_{sat}(L - \Delta L)}, & V_{DS} > V_{DSsat} \end{cases}, \quad (9)$$

where

$$V_{DSsat} = \frac{(V_{GS} - V_T)E_{sat}L}{(V_{GS} - V_T) + E_{sat}L}. \quad (10)$$

An important nuance for acoustic resonators is that both saturation velocity and change in mobility (piezoresistive effect) are related to the change in carrier effective mass caused by the acoustic deformation of the crystal lattice—saturation velocity by $m^{*-1/2}$ and mobility by a factor between $m^{*-1/2}$ and $m^{*-5/2}$ depending on doping (Supplementary Section 2 provides a detailed analysis). This relation means that although d.c. may saturate, the a.c. piezoresistive effect can still change the drain current to an extent, even in the saturation region. For this reason, a compound model is utilized that incorporates velocity saturation in the calculation of direct drain current but allows mobility to freely vary for a.c. calculations. Under this approach, the contribution to RF output from both electrostatic forces and mobility modulation should scale linearly with the drain current. The contribution from any threshold-voltage shift is seen to be related to drain bias only in the linear regime and is scaled by the impact of mobility and capacitance changes. In the saturation regime, on the other hand, the threshold-voltage shift is

primarily a function of gate bias and is modified by drain bias only through channel-length modulation. These expressions for ΔI_d represent one half of the device transfer function g_{mdd} (equation (1)), with the other half being given by the voltage-to-strain conversion and subsequent strain confinement/resonance. Although the direct measurement of strain in the solid-state resonator in FEOL poses a challenge, all three of these aspects are subsequently investigated using the measured electrical results.

Analysis of design variations

The d.c. results, shown as an example for the 80-nm-gate-length device (A1; Supplementary Section 6), indicate that the sense transistors in all the devices were working as intended. The large current values of approximately 2 mA when the gate and drain are biased at V_{dd} are due to the parallel d.c. connection of the two sense transistors and large effective width of the individual transistors, where 40 fins span the resonant cavity (in the y direction) and are electrically connected in parallel.

Although the d.c. results were similar for all the devices (outside the expected differences due to gate-length variations), resonance-mode confinement was highly dependent on the design variations studied. A comparison of their differential transconductance spectra are shown in Fig. 4 along with the dispersion relations of the 80 and 106 nm devices with Mx PnC and Cx plates. From these data, it is evident that PnC confinement in the Mx layers results in a significantly improved Q factor and maximum transconductance. An offset in resonant frequencies between the simulated and experimental devices shows the challenge in simulating commercial CMOS devices, where a plethora of materials and complex geometries introduce opportunities for simulation error. Also visible is the role that the type of termination has in defining the centre frequency of nearby spurious modes in the device. This is not easily studied in simulation due to the computational intensity of simulating the full structure, highlighting the importance of experimental design splits in optimizing the performance.

Analysis of variance (ANOVA) was used to quantify the impact of these variations in device design on the spectrum of acoustic modes. Such an analysis including several modes does not give an exact value for mode frequency, Q factor or amplitude, but rather compares the average value that might be expected based on the selected design parameters. This analysis indicates an increased average transconductance in gradual transition devices (352 nS) versus abruptly terminated ones (302 nS), with a corresponding increase in the average Q factor (32 versus 24, respectively). In addition to this enhancement, the average resonance centre frequency was shown to slightly decrease from 11.29 to 11.16 GHz, driven by the downward shift in the left-most peak of the high- Q cluster of modes seen in PnC-confined devices.

The investigation of PnC confinement showed no significant change in the centre frequency of the modes, but it did show significantly improved average transconductance (204, 379 and 451 nS) and Q factor (20, 38 and 44, respectively) with increasing layers of PnC confinement. These trends are highlighted in Supplementary Fig. 10 along with an example of the peak-fitting results used for parameter extraction.

A comparison between the 80- and 106-nm-gate-length devices showed increasing average mode frequency at shorter gate lengths (11.66 versus 10.71 GHz, respectively), as expected given that this alters the resonator unit-cell dimensions. The complete ANOVA results are provided in Supplementary Table 1, where the centre frequency, Q factor and height of the resonant peaks in g_{mdd} are compared for the three design splits.

As the device with the highest performance, resonator A2 was selected for further analysis, with the maximum transconductance of the 11.75 GHz mode examined as a function of device biasing. This was done at a drive bias of V_{dd} , as g_{mdd} was seen to linearly

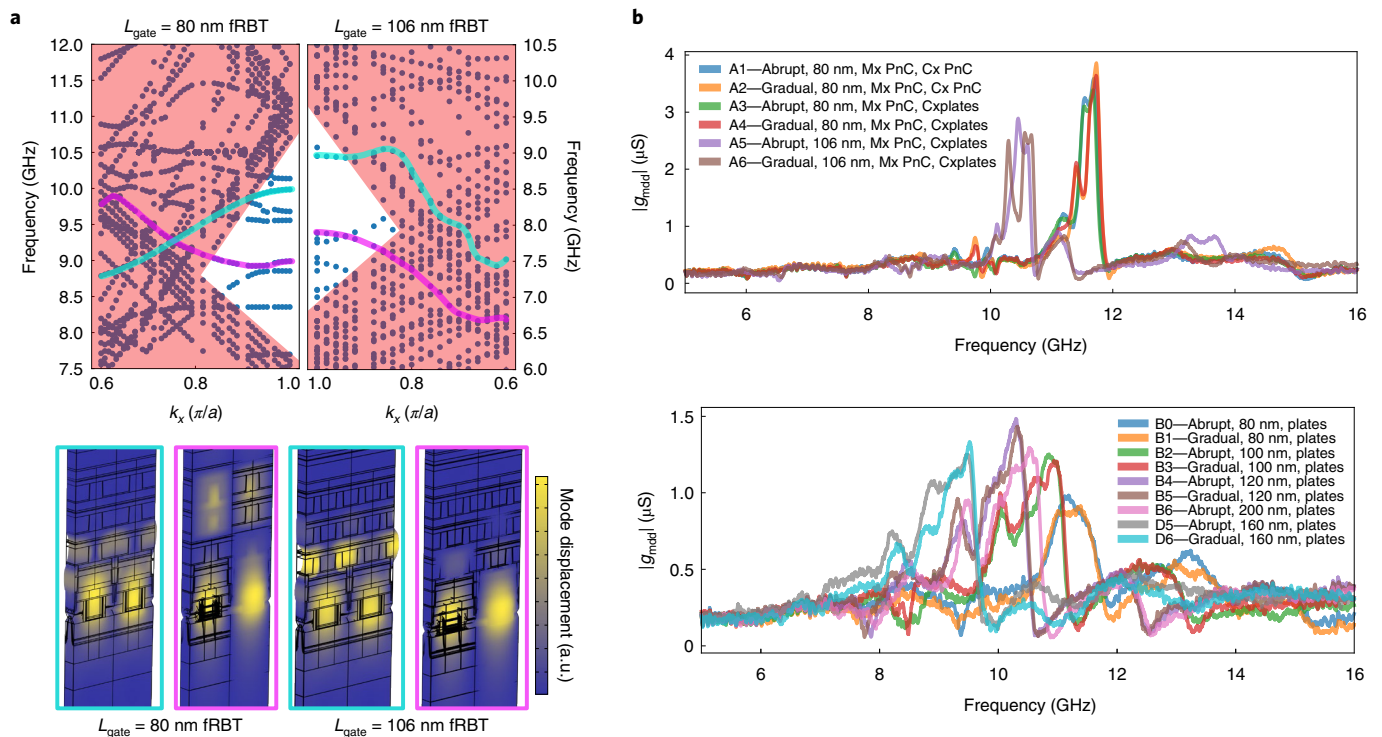


Fig. 4 | Experimental comparison of resonator designs. **a**, Simulated dispersion relation of 80- and 106-nm-gate-length unit cells with Mx PnC and Cx plates (A3–A6). The regions of Mx and Cx modes are shaded in red, corresponding to the propagating mode shown in Fig. 2f. This is shifted down in frequency for the longer-gate-length device due to the smaller absolute momentum at the X point. Additional modes along reciprocal lattice vector ΓX (Supplementary Fig. 4) are caused by the finite number of metal layers in the device unit cell, unlike the infinite periodicity assumed in the BEOL simulation. Modes with high-elastic-energy percentage confined in the silicon fin (Supplementary Fig. 5) are highlighted for both devices. As expected from the simulations of BEOL confinement schemes, the 106 nm device with Mx 76–32 PnC shows fewer BEOL waveguided modes. **b**, Experimentally measured differential transconductance (0 dBm, $V_{\text{drain}} = 0.8 \text{ V}$, $V_{\text{gate}} = 0.8 \text{ V}$ and $V_{\text{drive}} = 0.8 \text{ V}$), separated by devices with Mx PnC (top) and Mx plates (bottom). Despite the discrepancy in absolute frequency, the simulated relative frequency offset between the modes and across the devices matches well with the experiment. The sudden increase in resonance frequency for the $L_{\text{gate}} = 200 \text{ nm}$ device may indicate that a harmonic mode is being driven, with the first-order mode falling below the range of confined frequencies.

increase with the increase in metal–oxide–semiconductor capacitance at higher drive bias (Supplementary Section 6). The dependence of g_{mdd} on sense transistor biasing (Fig. 5) highlights that device transconductance, as expected, is modulated in a manner consistent with piezoresistive and bandgap modulation. Although the transistor parameters are of the correct order of magnitude in the reported data fit, they slightly vary from real-world values due to the simplified model used. For example, the square-law model does not accurately capture the subthreshold (accumulation and weak inversion) behaviour, and thus, the fit favours a slightly lower V_T to more closely fit the bias currents near zero. This, in turn, leads to an overestimation of current at higher biases, which is compensated by a lower than expected value for mobility and a slightly larger equivalent oxide thickness. On the a.c. side, the fit is hindered by the presence of a noise floor in the S-parameter measurements that may obscure the lower peak levels. This, along with the poor near-threshold characteristics of the square-law model, contributes to the fitting error at lower values of g_{mdd} . Future devices incorporating ferroelectric drive capacitors would mitigate this issue by greatly increasing the efficiency of electromechanical conversion²⁵ and hence boosting the vibration amplitude and/or lowering power consumption. Moving away from the square-law model to a more advanced model such as that derived in another work²⁶ that captures all the regions of operation may decrease this error. Similarly, adopting band-structure simulations of silicon as a result of acoustic deformation could provide a unified source of mobility

and threshold-voltage changes in the transistor, at the expense of increased computational requirements.

For n-type metal–oxide–semiconductor devices oriented in the $\langle 110 \rangle$ direction, the negative piezoresistive coefficients ensure that the contribution of threshold-voltage shift and mobility is additive. If fRBT devices are implemented with p-type metal–oxide–semiconductor devices or in processes with different fin orientations, care should be taken to ensure that the dominant stress-dependent effects do not compete with each other. This may not be as much of an issue for long-channel resonant body transistor devices, as piezoresistive modulation dominates for long-channel devices that are not constrained by the supply voltage.

The highest-magnitude peak fit occurred in device A2 ($L_{\text{gate}} = 80 \text{ nm}$, gradually terminated, dual PnC) at 11.73 GHz with a differential transconductance of $4.49 \mu\text{S}$ and $Q = 69.8$, for an $f \times Q$ product of 8.19×10^{11} at drain, gate and drive biases of 0.6, 0.8 and 0.8 V, respectively. Although previously demonstrated unreleased resonators in the 32 nm silicon-on-insulator (SOI) process have achieved an $f \times Q$ product of 3.8×10^{13} with phononic confinement at 3.3 GHz, these 14 nm devices exhibit 50 times higher transconductance and show an almost three times improvement in Q over a similar frequency-measured mode in 32 nm SOI devices^{27,28}. Compared with some contemporary resonators in the X-band and adjacent K_u -band (12–18 GHz; Table 1), the unreleased devices in this work achieve moderate $f \times Q$ in an area smaller than comparable released devices. This, combined with the fact that the devices are

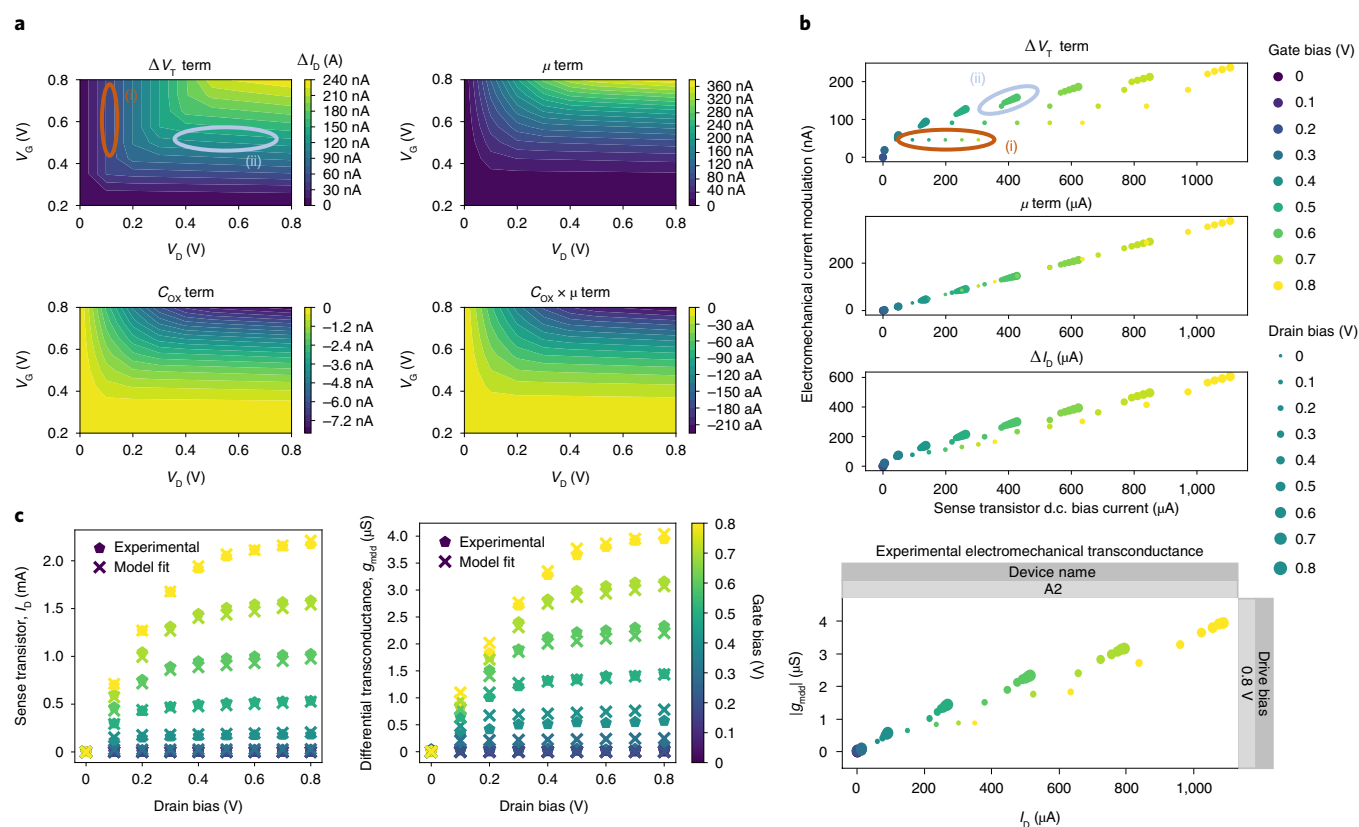


Fig. 5 | Bias dependence of active sensing. **a**, Simulated contributions to ΔI_d from bandgap modulation (threshold voltage), piezoresistive modulation (mobility), electrostatic modulation (oxide capacitance) and cross-term. For short-channel devices that are constrained by supply voltage, bandgap and piezoresistive modulation are of similar magnitudes and dominate over the electrostatic terms. **b**, These two terms, along with the overall drain current modulation, are plotted against the d.c. bias current of the sense transistor (x axis) for the simulated (top) and experimental (bottom) devices. The gate bias is shown by the marker colour (blue to yellow) and ranges from 0.0 to 0.8 V in steps of 0.1 V. The drain bias is represented by the marker size, moving from small to large as the bias increases from 0.0 to 0.8 V in steps of 0.1 V. The large cluster of points with equal gate biases and similar drain currents indicate saturation-mode operation for those bias conditions with channel-length modulation. The mobility term is linear with drain current, whereas the threshold-voltage term due to bandgap modulation has both a flat region (i) in the linear regime with no V_{GS} dependence for constant V_{DS} and a slight V_{DS} dependence (ii) for constant V_{GS} in the saturation regime. The experimental data roughly show a linear dependence of drain current on gate voltage (a hallmark of velocity saturation²² versus the V_{GS}^2 dependence of the long-channel model). Some deviation between the model fit and experimental results can be seen at high drain bias and low gate bias, which may be indicative of mobility degradation due to vertical fields, which is not currently modelled. Additionally, the fit becomes worse when approaching the subthreshold, due to the abrupt cutoff in the drain current at V_T in the square-law model. Otherwise, the experimental results show a similar shape to that of the simulated device, indicating the dominance of both piezoresistive and bandgap modulation in the experimental resonator. **c**, Model fit to the experimental results ($\mu = 50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$; equivalent oxide thickness, 1.2 nm; $V_T = 0.24 \text{ V}$; $v_{sat} = 2.72 \times 10^7 \text{ cm s}^{-1}$; $\lambda = 0.24$; $W = 3.9 \mu\text{m}$; total stress, 0.97 MPa). A basin-hopping algorithm is used to find a global minimum fit for the d.c. transistor parameters, which are then fixed for the a.c. fit achieved by varying the stress.

integrated in the FEOL of a commercial CMOS technology node, opens the door for tight logic integration with minimum routing (and associated parasitics). Additional optimizations to the PnC and termination, although challenging due to process design rules, may further boost the Q factor of these devices. Furthermore, the incorporation of PnC confinement in longer gate lengths would enable this enhanced performance to be achieved across the IEEE X-band.

Conclusions

We have reported unreleased resonant fin transistors fabricated in standard 14 nm FinFET technology. An analytical model was developed that predicts resonator performance across sense transistor biasing conditions, using a combined velocity-saturated current at d.c. and unsaturated mobility variation at a.c. This highlights how the acoustic perturbation of carrier effective mass simultaneously modulates the saturation velocity and mobility. PnC confinement, which was experimentally shown to be the most important parameter in improving the unreleased resonator performance

(an improvement on average of 2.2 times), provides a considerable opportunity for integrating acoustic devices into standard CMOS platforms. Our highest performing resonator—a gradually terminated 80-nm-gate-length device with both Mx and Cx PnC confinement—exhibits a transconductance amplitude of $4.49 \mu\text{S}$ and Q of 69.8, in the 11.73 GHz mode, resulting in an $f \times Q$ product of 8.2×10^{11} . This technology—combined with advances in CMOS-compatible ferroelectric and piezoelectric thin films—could be used to develop compact, low-cost, CMOS-integrated and electrically controllable resonators that require no additional packaging.

Characterization methods

Device measurement. An overview of the entire data pipeline is depicted in Supplementary Fig. 6. This process begins with S-parameter measurements taken at room temperature and pressure, with an input power of -10 dBm using an Agilent Technologies N5225a PNA instrument, with biasing provided by three Keithley 2400 source measure units (Supplementary Fig. 7). All the four devices were

Table 1 | Comparison with contemporaneously reported X-band and K_u-band (8–18 GHz) resonators

Reference	f_0 (GHz)	Q	f_0Q	Technology	Released?	Area (μm^2)
This work	11.73	69.8	8.2×10^{11}	Commercial 14LPP	No	135
28	11.5	24	2.8×10^{11}	Commercial 32SOI	No	15
25	18.01	360	6.48×10^{12}	Custom HZO	Freestanding	36
36	8.8	750	6.6×10^{12}	Custom AlN	Yes	6,500
6	11.1	615	6.8×10^{12}	Custom AlN	Yes	675
37	13.0	282	3.7×10^{12}	Custom LiNbO ₃	Yes	2,000
38	14.5	400	5.8×10^{12}	Printed circuit board microstrip	–	27,000,000

connected via General Purpose Interface Bus and synchronized via published Python3 scripts^{29,30}. WinCal XE 4.7 software (FormFactor) was used to facilitate the pre-measurement calibration, and hybrid Line-Reflect-Reflect-Match-Short-Open-Load-Reciprocal calibration was performed using an impedance standard substrate (ISS 129-246). Infinity ground-signal-signal-ground probes were used to allow for a compact biasing scheme, saving die real estate at the expense of increased cross-talk between the adjacent signal lines. Gate bias for the sense transistors was provided via a separate d.c. needle probe.

Measurement data post-processing. The acquired Touchstone files were first analysed using scikit-rf, which was used to perform open de-embedding and transform the single-ended parameters collected into their mixed-mode equivalent matrices³¹. From these, g_{mdd} was extracted to allow for the analysis of the designed differential mode. The magnitude of g_{mdd} for each sample at a bias of $V_{\text{drain}} = 0.6\text{ V}$, $V_{\text{gate}} = 0.8\text{ V}$ and $V_{\text{drive}} = 0.8\text{ V}$ was modelled as a collection of Gaussian peaks and fit via Lmfit using the Levenberg–Marquardt algorithm with initial guesses for frequency and peak height provided via user input through matplotlib's ginput method³². These preliminary fits were then used as the initial conditions for the remainder of the 450 collected measurements taken at drain biases of 0.2, 0.4 and 0.6 V; drive biases of 0, 0.2, 0.4, 0.6 and 0.8 V; and sense FET gate biases of 0 and 0.8 V. These were again fit via Lmfit and parallelized using Dask³³. Due to the noisy nature of the data, with varying spectra between devices, a number of constraints were added to improve the fitting accuracy over all the design variations. The fitting was weighted by the g_{mdd} amplitude to emphasize the primary peaks over smaller spurious modes and background noise. Variation in peak standard deviation between the biases was constrained to two times the original standard deviation, reflecting the fact that Q is a function of the physical mode confinement. The centre frequency for each sample was constrained to a maximum of 5% deviation as a function of bias to improve the fitting accuracy and reflect the fact that mode shape—and thus the frequency of operation—again is primarily dictated by device geometry and not biasing.

Design variation analysis. The extracted peak properties were analysed in SAS JMP Pro 14 statistical discovery software to investigate the relationship between the splits in device design and variation in performance as a function of device bias³⁴. Before the analysis was carried out, high-error peak fits were eliminated (mean square error, >0.025 ; $\approx 5\%$ of the data overall). The device splits (Fig. 2) are not entirely orthogonal due to a variety of constraints in device design related to the PnC and gate lengths. Thus, one-way ANOVA was used on subsets of the experimental devices rather than trying to fit a multidimensional model to the entire sample set. To increase the number of statistical samples (and thus the chance of significance), all the bias combinations for each device were included in

the analysis. For termination, this process is straightforward as there exists an abrupt and gradually terminated copy of every device, resulting in a comparison of all the devices. To investigate PnC confinement, the analysis was limited to designs with 80 nm gate length (A1–A4 and B0–B1) and the confinement treated as a three-level categorical factor.

Compared with the other factors studied, L_{gate} is unique in that it is the primary design variable for selecting the centre frequency due to the mode being defined by source/drain spacing. This means that the different values studied dramatically change the cavity shape and thus all the peaks detected in the studied frequency span of 9.5–13.5 GHz cannot be used in the analysis, as they are not present in this range in all the devices. To overcome this, a much smaller comparison of A3 and A4 ($L_{\text{gate}} = 80\text{ nm}$) to A5 and A6 ($L_{\text{gate}} = 106\text{ nm}$) was performed using only the prominent modes with transconductance above 500 nS and Q above 25 that were present towards the centre of the spectra. The downside of this approach is that the gate length is confounded with a change in Mx PnC design that is necessary for the different device geometries due to challenges in design rules. Despite this, the fact that the confinement method showed no significant change in centre frequency for 80 nm devices points towards this shift being dominated by gate length, as expected.

Transistor modelling. The examination of expected device performance using the derived analytical model was performed in Python. The contribution for each of the three components (bandgap, mobility and capacitance modulation) was taken as the difference between the positive- and negative-stress components. Lmfit was used to perform the optimization routine, using a basin-hopping algorithm to find a global minimum for d.c. The fit of g_{mdd} was performed using the Levenberg–Marquardt algorithm. The simplified one-dimensional model of a 3D transistor led to substantial cross-correlation between the stress directional components; however, the magnitude of the total stress remained relatively constant across the fit iterations.

Data availability

Experimentally measured S-parameter and peak-fitting data are available at <https://doi.org/10.5281/zenodo.5899507> (ref. ³⁵). Device layouts subject to GlobalFoundries process design kit non-disclosure agreement are available from the corresponding authors on reasonable request and with permission from GlobalFoundries.

Code availability

All code used in device analysis is available at <https://doi.org/10.5281/zenodo.5899507> (ref. ³⁵). ANOVA analysis was performed in JMP software³⁴. All the other experimental analysis was performed with Python scripts.

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References

- GlobalFoundries. Optimized for AI accelerator applications, GLOBALFOUNDRIES 12LP+ FinFET solution ready for production. <https://gf.com/press-release/optimized-ai-accelerator-applications-globalfoundries-12lp-finet-solution-ready> (2020).
- Decadal Plan for Semiconductors. (Semiconductor Research Corporation, 2021). <https://www.src.org/about/decadal-plan/>
- Wang, J. et al. A film bulk acoustic resonator based on ferroelectric aluminum scandium nitride films. *J. Microelectromech. Syst.* **29**, 741–747 (2020).
- He, Y., Bahr, B., Si, M., Ye, P. & Weinstein, D. A tunable ferroelectric based unreleased RF resonator. *Microsyst. Nanoeng.* **6**, 8 (2020).
- Lu, R., Yang, Y., Link, S. & Gong, S. Enabling higher order Lamb wave acoustic devices with complementarily oriented piezoelectric thin films. *J. Microelectromech. Syst.* **29**, 1332–1346 (2020).
- Assylbekova, M. et al. 11 GHz lateral-field-excited aluminum nitride cross-sectional Lamé mode resonator. In *2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF)* 1–4 (IEEE, 2020).
- Yang, S. & Hanzo, L. Fifty years of MIMO detection: the road to large-scale MIMOs. *IEEE Commun. Surveys Tuts* **17**, 1941–1988 (2015).
- Fedder, G. K., Howe, R. T., Liu, T. K. & Quevy, E. P. Technologies for cofabricating MEMS and electronics. *Proc. IEEE* **96**, 306–322 (2008).
- Chen, C., Li, M., Zope, A. A. & Li, S. A CMOS-integrated MEMS platform for frequency stable resonators—part I: fabrication, implementation, and characterization. *J. Microelectromech. Syst.* **28**, 744–754 (2019).
- Riverola, M., Sobreviela, G., Torres, F., Uranga, A. & Barniol, N. Single-resonator dual-frequency BEOL-embedded CMOS-MEMS oscillator with low-power and ultra-compact TIA core. *IEEE Electron Device Lett.* **38**, 273–276 (2017).
- Bahr, B., Marathe, R. & Weinstein, D. Phononic crystals for acoustic confinement in CMOS-MEMS resonators. In *2014 IEEE International Frequency Control Symposium (FCS)* 1–4 (IEEE, 2014).
- Bahr, B., Marathe, R. & Weinstein, D. Theory and design of phononic crystals for unreleased CMOS-MEMS resonant body transistors. *J. Microelectromech. Syst.* **24**, 1520–1533 (2015).
- Razavi, B. Jitter-power trade-offs in PLLs. *IEEE Trans. Circuits Syst. I, Reg. Papers* **68**, 1381–1387 (2021).
- Nikonov, D. E., Young, I. A. & Bourianoff, G. I. Convolutional networks for image processing by coupled oscillator arrays. Preprint at <https://arxiv.org/abs/1409.4469> (2014).
- Nikonov, D. E. et al. Coupled-oscillator associative memory array operation for pattern recognition. *IEEE J. Explor. Solid-State Computat.* **1**, 85–93 (2015).
- Corti, E. et al. Coupled VO₂ oscillators circuit as analog first layer filter in convolutional neural networks. *Front. Neurosci.* **15**, 628254 (2021).
- GlobalFoundries. 12LP: 12nm FinFET technology <https://www.globalfoundries.com/sites/default/files/product-briefs/pb-12lp-11-web.pdf> (2018).
- Trentzsch, M. et al. A 28nm HKMG super low power embedded NVM technology based on ferroelectric FETs. In *2016 IEEE International Electron Devices Meeting (IEDM)* 11.5.1–11.5.4 (IEEE, 2016).
- He, Y., Bahr, B., Si, M., Ye, P. & Weinstein, D. Switchable mechanical resonance induced by hysteretic piezoelectricity in ferroelectric capacitors. In *2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII)* 717–720 (IEEE, 2019).
- COMSOL Multiphysics Versions 5.5 (COMSOL). <https://www.comsol.com/>
- Joannopoulos, J. D., Johnson, S., Winn, J. & Meade, R. *Molding the Flow of Light* 2nd edn (Princeton Univ. Press, 2008).
- Tsividis, Y. & McAndrew, C. *Operation and Modeling of the MOS Transistor* 3rd edn (Oxford Univ. Press, 2010).
- BSIM Group. <http://bsim.berkeley.edu/>
- Rawat, U., Bahr, B. & Weinstein, D. Analysis and modeling of an 11.8GHz fin resonant body transistor in a 14nm FinFET CMOS process. *IEEE Trans. Ultrason., Ferroelectr., Freq. Control* **69**, 1399–1412 (2022).
- Hakim, F., Tharpe, T. & Tabrizian, R. Ferroelectric-on-Si super-high-frequency fin bulk acoustic resonators with Hf_{0.5}Zr_{0.5}O₂ nanolaminated transducers. *IEEE Microw. Wireless Compon. Lett.* **31**, 701–704 (2021).
- Taur, Y., Liang, X., Wang, W. & Lu, H. A continuous, analytic drain-current model for DG MOSFETs. *IEEE Electron Device Lett.* **25**, 107–109 (2004).
- Bahr, B., Daniel, L. & Weinstein, D. Optimization of unreleased CMOS-MEMS RBTs. In *2016 IEEE International Frequency Control Symposium (IFCS)* 1–4 (IEEE, 2016).
- Marathe, R. et al. Resonant body transistors in IBM's 32nm SOI CMOS technology. *J. Microelectromech. Syst.* **23**, 636–650 (2014).
- Anderson, J. & Weinstein, D. PyMeasRF: automating RF device measurements using Python. *Zenodo* <https://zenodo.org/record/3346201> (2019).
- Anderson, J. PyMeasRF. *GitHub* <https://github.com/JAnderson419/PyMeasRF> (2020).
- Scikit-rl Developers. Scikit-rl <http://scikit-rl.org/index.html> (2020).
- LMFIT: non-linear least-squares minimization and curve-fitting for Python. <https://lmfit.github.io/lmfit-py/> (2020).
- Dask: scalable analytics in Python. <https://dask.org/> (2020).
- JMP. https://www.jmp.com/en_us/home.html (2019).
- Anderson, J., He, Y., Bahr, B. & Weinstein, D. Dataset for 'X-band fin resonant body transistors in 14nm CMOS technology'. *Zenodo* <https://zenodo.org/record/5899507> (2022).
- Chen, G. & Rinaldi, M. High-Q X band aluminum nitride combined overtone resonators. In *2019 Joint Conference of the IEEE International Frequency Control Symposium and European Frequency and Time Forum (EFTF/IFC)* 1–3 (IEEE, 2019).
- Yang, Y., Lu, R., Gao, L. & Gong, S. 10–60-GHz electromechanical resonators using thin-film lithium niobate. *IEEE Trans. Microw. Theory Techn.* **68**, 5211–5220 (2020).
- Abouyoussef, M. S., El-Tager, A. M. & El-Ghitani, H. Quad spiral microstrip resonator with high quality factor. In *2018 35th National Radio Science Conference (NRSC)* 6–13 (IEEE, 2018).
- Srivastava, A. et al. A mmWave oscillator design utilizing high-Q active-mode on-chip MEMS resonators for improved fundamental limits of phase noise. Preprint at <https://arxiv.org/abs/2107.01953> (2021).

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Author contributions

J.A. performed the device measurements, analysis, 3D PnC modelling and electrical modelling, as well as led the manuscript preparation. Y.H. drafted the sections on phononic confinement and cavity termination schemes and performed simulations related to device acoustic design. B.B. designed the devices and managed the tapeout of the resonators measured, as well as the construction of an initial COMSOL model for device simulation. D.W. provided feedback and guidance to the authors across device design, measurement and manuscript preparation.

Competing interests

B.B. was employed as an intern by GlobalFoundries during the initial tapeout of the reported devices. The other authors declare no competing interests.

Additional information

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